PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-223297

(43)Date of publication of application : 17.08.2001

(51)Int.Cl. H01L 23/12
H01L 23/28
H01L 23/52
// H01L 25/065
H01L 25/07
H01L 25/18
H01L 25/10
H01L 25/11

(21)Application number : 2000-068986

(22)Date of filing : 13.03.2000

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(30)Priority

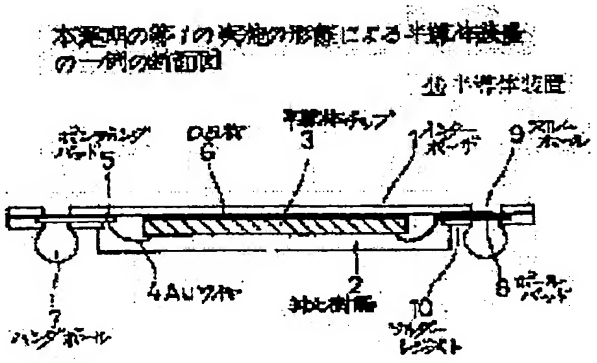
Priority number : 11340816 Priority date : 30.11.1999 Priority country : JP

(54) SEMICONDUCTOR DEVICE, ITS MANUFACTURING METHOD AND ITS LAMINATING METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device and its manufacturing method which can improve the packaging density as a three-dimensional structure by laminating a plurality of semiconductor devices.

SOLUTION: A semiconductor chip is mounted on one side of an interposer 1, and the electrode of the semiconductor chip 3 is connected to a bonding pad 5. A soldering ball 7 is provided on a ball pad 8 connected to the bonding pad 5. A through-hole 9 is provided on the interposer 1 on the side opposite to the soldering ball on the ball pad 8. The height of the soldering ball is made higher than that of the sealing resin 2 of the semiconductor chip 3.



LEGAL STATUS

[Date of request for examination] 25.11.2003

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

CLAIMS

[Claim(s)]
[Claim 1] On the 1st [of the rewiring substrate which has a semiconductor device, the 1st field in which this semiconductor device is carried and the 2nd field of the opposite side of this 1st field, and this rewiring substrate] field The electrode pad which has been arranged around said semiconductor device and was electrically connected with said semiconductor device, The semiconductor device characterized by having consisted of a projection electrode prepared on this electrode pad, and a through tube from said 2nd field of said rewiring substrate to said electrode pad, and making the height from said 1st field of said projection electrode higher than the closure height from said 2nd field of said semiconductor device.
[Claim 2] On the 1st [of the rewiring substrate which has a semiconductor device, the 1st field in which this semiconductor device is carried, and the 2nd field of the opposite side of this 1st field, and this rewiring substrate] field The electrode pad which has been arranged around said semiconductor device and was electrically connected with said semiconductor device, It consists of a through tube from said 2nd field of said rewiring substrate to this electrode pad, and a projection electrode prepared in said electrode pad from this through tube side. The semiconductor device characterized by making the height from said 2nd field of said projection electrode higher than the closure height from said electrode pad of said semiconductor device.
[Claim 3] The semiconductor device which is a semiconductor device according to claim 1 or 2, carries out laminating immobilization of other semiconductor devices at said semiconductor device, and is characterized by closing in one.
[Claim 4] On the 1st [of the rewiring substrate which has the 1st field in which the 1st and 2nd semiconductor devices and these 1st semiconductor devices were carried, and the 2nd field in which this 2nd semiconductor device was carried, and this rewiring substrate] field On the 1st electrode pad which has been arranged around said 1st semiconductor device and was electrically connected with said 1st semiconductor device, and the 2nd [of said rewiring substrate] field The 2nd electrode pad which has been arranged around said 2nd semiconductor device and was electrically connected with said 2nd semiconductor device, The VIA hole which connects electrically said 1st electrode pad and said 2nd electrode pad, The semiconductor device characterized by having consisted of a projection electrode prepared in said 1st electrode pad or said 2nd electrode pad, and making the height of said projection electrode higher than the closure height of said 1st semiconductor device.
[Claim 5] It is the semiconductor device characterized by being a semiconductor device according to claim 4, and making said projection electrode higher than total with the closure height of said 1st semiconductor device, and the closure height of said 2nd semiconductor device.
[Claim 6] The semiconductor device which is a semiconductor device according to claim 4 or 5, carries out laminating immobilization of the 3rd semiconductor device at either, and is characterized by the thing of said 1st semiconductor device and said 2nd semiconductor device closed in one at least.
[Claim 7] It is the semiconductor device which it is a semiconductor device according to claim 4 or 5, and said 1st and 2nd semiconductor devices are connected to said 1st and 2nd electrode pads by wirebonding, and is characterized by the connecting location of the wire on said 1st electrode pad

having shifted from the connecting location of the wire on said 2nd electrode pad.

[Claim 8] The semiconductor device which is a semiconductor device which has the laminated structure which carried out the laminating of two or more semiconductor devices indicated by claim 1 thru/or 7, and was connected, and is characterized by the number of electrodes of the semiconductor device of the top in a laminated structure differing from the number of electrodes of a lower semiconductor device.

[Claim 9] It is the manufacture approach of a semiconductor device that the 1st semiconductor device was carried in the 1st field of a rewiring substrate, and the 2nd semiconductor device was carried in the 2nd field of the opposite side of this 1st field. Said 1st semiconductor device is carried in the 1st field of said rewiring substrate. Said rewiring substrate Inside-out, Said rewiring substrate is laid on the fixture which has the buffer member which has the crevice in which said 1st semiconductor device is held, and supports said 1st semiconductor device in this crevice. The manufacture approach of the semiconductor device characterized by having each phase of carrying said 2nd semiconductor device in the 2nd field of said rewiring substrate.

[Claim 10] A rewiring substrate and the semiconductor device protected by the package while being carried in the center of this rewiring substrate, The projection electrode arranged in the periphery location of this semiconductor device of said rewiring substrate, Two or more semiconductor devices which have the electrode pad arranged so that said projection electrode arrangement side and opposite side side of said rewiring substrate might be countered with said projection electrode While arranging said semiconductor device in the laminating approach of the semiconductor device which carries out a laminating by joining said projection electrode and said electrode pad so that said projection electrode may serve as the bottom to the direction of a laminating The laminating approach of the semiconductor device characterized by having the flux arrangement process which imprints said flux on said projection electrode using an imprint head with the fluxing section by which flux is applied only to the arrangement location of said projection electrode, and a corresponding location.

[Claim 11] A rewiring substrate and the semiconductor device protected by the package while being carried in the center of this rewiring substrate, The projection electrode arranged in the periphery location of this semiconductor device of said rewiring substrate, Two or more semiconductor devices which have the electrode pad arranged so that said projection electrode arrangement side and opposite side side of said rewiring substrate might be countered with said projection electrode In the laminating approach of the semiconductor device which carries out a laminating by joining said projection electrode and said electrode pad To the flux feed zone material which has the flux loading section by which only the location corresponding to the arrangement location of said projection electrode was loaded with flux The laminating approach of the semiconductor device characterized by having the flux arrangement process which arranges said flux on said projection electrode by conveying said semiconductor device in the condition that said projection electrode serves as the bottom to the direction of a laminating, and immersing said projection electrode in said flux loading section.

[Translation done.]

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the manufacture approach of a semiconductor device and a semiconductor device, and relates to the manufacture approach of a suitable semiconductor device to carry out the laminating of two or more semiconductor devices, consider as the three-dimensional structure, and aim at improvement in packaging density especially, and a semiconductor device.
[0002] A miniaturization and thin shape-ization are demanded also of the semiconductor device used for electronic equipment with thin-shape[the miniaturization of electronic equipment, lightweight-izing, and]-izing. The package of a semiconductor device is shifting to the BGA (ball grid array) mold package or CSP (chip-size package) which has arranged the external connection terminal in the shape of an area array at the base of a package in the four directions from QFP for surface mounts to which the terminal extended in the shape of a gull wing that such a demand should be coped with.
[0003] In such a semiconductor package, a semiconductor chip is mounted in a rewiring substrate (INTAPOZA), and many the so-called fan-out type which has arranged the terminal for external connection around a semiconductor chip by INTAPOZA of packages are used.
[0004]
[Description of the Prior Art] Drawing 1 is the sectional view of the semiconductor device of the conventional fan-out mold. In drawing 1 , a semiconductor chip 3 is carried in INTAPOZA 1 which consists of a polyimide substrate or a glass epoxy group plate, and the closure is carried out with closure resin 2. The semiconductor chip 3 is being fixed to INTAPOZA 1 by the DB material (bonding agent) 6 in the state of face up. The bonding pad 5 and the ball pad 8 are formed in the top face of INTAPOZA 1, and the circuit pattern connects, respectively.
[0005] The electrode and bonding pad 5 of a semiconductor chip 3 are connected by the Au wire 4. Moreover, in order to protect a semiconductor chip 3, the Au wire 4, and bonding pad 5 grade, the closure of the field in which the semiconductor chip 3 of INTAPOZA 1 was carried is carried out with the closure resin 2 which consists of epoxy system resin etc. A through hole (VIA hole) 9 is established in the location corresponding to the ball pad 8 and bonding pad 5 of INTAPOZA 1 from the inferior-surface-of-tongue side, and the pewter ball 7 is formed in the ball pad 8 and the bonding pad 5. Therefore, the semiconductor chip 3 is electrically connected to the pewter ball 7 which is an external connection terminal through INTAPOZA 1, and the pewter ball 7 is projected and formed in the inferior-surface-of-tongue side of INTAPOZA 1.
[0006] Drawing 2 is the sectional view of CSP (chip-size package) of the conventional flip chip mounting mold. In drawing 2 , the same sign is given to the same components as the component part shown in drawing 1 , and the explanation is omitted.
[0007] In drawing 2 , flip chip mounting of the semiconductor chip 3 is carried out in the state of the face down at INTAPOZA 1. That is, the semiconductor chip 3 has the bump 12 for connection, and the bump 12 for connection is connected to the bonding pad 5. It fills up with the under-filling material 11 between a semiconductor chip 3 and INTAPOZA 1, and the semiconductor chip 3 is being fixed to INTAPOZA 1. Like the semiconductor device shown in drawing 1 , a through hole (VIA hole) 9 is established in INTAPOZA 1, and the pewter ball 7 is projected and formed in the inferior-surface-of-tongue side of INTAPOZA 1.
[0008]
[Problem(s) to be Solved by the Invention] In the above-mentioned semiconductor package, most sizes of a package are reduced to the semi-conductor chip size by reducing the component-side product of PA&KEJI including a semiconductor chip. Therefore, it is necessary to think that two-dimensional

contraction of package structure has reached the limitation mostly, and to consider the miniaturization of a semiconductor device in three dimensions from now on. That is, it is becoming important how not only the component-side product of a semiconductor device but the mounting volume is made small.
[0009] This invention is made in view of an above-mentioned technical problem, and it aims at offering the semiconductor device which enabled mounting of a semiconductor device in three dimensions, and its manufacture approach by carrying out the laminating of the semiconductor device package according to easy structure, and unifying.
[0010]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, the semiconductor device by invention according to claim 1 On the 1st [of the rewiring substrate which has a semiconductor device, the 1st field in which this semiconductor device is carried, and the 2nd field of the opposite side of this 1st field, and this rewiring substrate] field The electrode pad which has been arranged around said semiconductor device and was electrically connected with said semiconductor device, It consists of a projection electrode prepared on this electrode pad, and a through tube from said 2nd field of said rewiring substrate to said electrode pad, and considers as the configuration which made the height from said 1st field of said projection electrode higher than the closure height from said 2nd field of said semiconductor device.
[0011] The semiconductor device by invention according to claim 2 on the 1st [of the rewiring substrate which has a semiconductor device, the 1st field in which this semiconductor device is carried, and the 2nd field of the opposite side of this 1st field, and this rewiring substrate] field The electrode pad which has been arranged around said semiconductor device and was electrically connected with said semiconductor device, It consists of a through tube from said 2nd field of said rewiring substrate to this electrode pad, and a projection electrode prepared in said electrode pad from this through tube side, and considers as the configuration which made the height from said 2nd field of said projection electrode higher than the closure height from said electrode pad of said semiconductor device.
[0012] Invention according to claim 3 is a semiconductor device according to claim 1 or 2, carries out laminating immobilization of other semiconductor devices at said semiconductor device, and is taken as the configuration closed in one.
[0013] Invention according to claim 4 on the 1st [of the rewiring substrate which has the 1st field in which the 1st and 2nd semiconductor devices and these 1st semiconductor devices were carried, and the 2nd field in which this 2nd semiconductor device was carried, and this rewiring substrate] field On the 1st electrode pad which has been arranged around said 1st semiconductor device and was electrically connected with said 1st semiconductor device, and the 2nd [of said rewiring substrate] field The 2nd electrode pad which has been arranged around said 2nd semiconductor device and was electrically connected with said 2nd semiconductor device, The VIA hole which connects electrically said 1st electrode pad and said 2nd electrode pad, It consists of a projection electrode prepared in said 1st electrode pad or said 2nd electrode pad, and considers as the configuration which made the height of said projection electrode higher than the closure height of said 1st semiconductor device.
[0014] Invention according to claim 5 is a semiconductor device according to claim 4, and considers said projection electrode as the configuration made higher than total with the closure height of said 1st semiconductor device, and the closure height of said 2nd semiconductor device.
[0015] Invention according to claim 6 is a semiconductor device according to claim 4 or 5, and is taken as the configuration of said 1st semiconductor device and said 2nd semiconductor device which carried out laminating immobilization of the 3rd semiconductor device at least at either, and was closed in one.
[0016] Invention according to claim 7 is a semiconductor device according to claim 4 or 5, said 1st and 2nd semiconductor devices are connected to said 1st and 2nd electrode pads by wirebonding, and the connecting location of the wire on said 1st electrode pad is considered as the configuration which has shifted from the connecting location of the wire on said 2nd electrode pad.
[0017] Invention according to claim 8 is a semiconductor device which has the laminated structure

which carried out the laminating of two or more semiconductor devices indicated by claim 1 thru/or 7, and was connected, and is taken as the configuration from which the number of electrodes of the semiconductor device of the top in a laminated structure and the number of electrodes of a lower semiconductor device differ.

[0018] As for invention according to claim 9, the 1st semiconductor device is carried in the 1st field of a rewiring substrate. It is the manufacture approach of a semiconductor device that the 2nd semiconductor device was carried in the 2nd field of the opposite side of this 1st field. Said 1st semiconductor device is carried in the 1st field of said rewiring substrate. Said rewiring substrate Inside-out, Said rewiring substrate is laid on the fixture which has the buffer member which has the crevice in which said 1st semiconductor device is held, and supports said 1st semiconductor device in this crevice, and it considers as the configuration which has each phase of carrying said 2nd semiconductor device in the 2nd field of said rewiring substrate.

[0019] The semiconductor device protected by the package while invention according to claim 10 was carried in the center of a rewiring substrate and this rewiring substrate, The projection electrode arranged in the periphery location of this semiconductor device of said rewiring substrate, Two or more semiconductor devices which have the electrode pad arranged so that said projection electrode arrangement side and opposite side side of said rewiring substrate might be countered with said projection electrode While arranging said semiconductor device in the laminating approach of the semiconductor device which carries out a laminating by joining said projection electrode and said electrode pad so that said projection electrode may serve as the bottom to the direction of a laminating It considers as the configuration which has the flux arrangement process which imprints said flux on said projection electrode using an imprint head with the fluxing section by which flux is applied only to the arrangement location of said projection electrode, and a corresponding location.

[0020] The semiconductor device protected by the package while invention according to claim 11 was carried in the center of a rewiring substrate and this rewiring substrate, The projection electrode arranged in the periphery location of this semiconductor device of said rewiring substrate, Two or more semiconductor devices which have the electrode pad arranged so that said projection electrode arrangement side and opposite side side of said rewiring substrate might be countered with said projection electrode In the laminating approach of the semiconductor device which carries out a laminating by joining said projection electrode and said electrode pad To the flux feed zone material which has the flux loading section by which only the location corresponding to the arrangement location of said projection electrode was loaded with flux Said semiconductor device is conveyed in the condition that said projection electrode serves as the bottom to the direction of a laminating, and it considers as the configuration which has the flux arrangement process which arranges said flux on said projection electrode by immersing said projection electrode in said flux loading section.

[0021] Each above-mentioned means acts as follows.

[0022] According to invention according to claim 1, a through tube is prepared in INTAPOZA on the background of an electrode pad in which the projection electrode was prepared, and the background side (field of a projection electrode and the opposite side) of an electrode pad is exposed within a through tube. Moreover, since the height of a projection electrode is higher than the closure height of a semiconductor device, when carrying out the laminating of the semiconductor device of the same structure, the projection electrode of an upper semiconductor device can be connected to the electrode pad in the through tube of a lower semiconductor device. At this time, the part to which the closure of the semiconductor device of an upper semiconductor device was carried out is held in the space formed with the projection electrode between the rewiring substrate of an upper semiconductor device, and the rewiring substrate of a lower semiconductor device. Therefore, only a projection electrode can prescribe connection of each semiconductor device and the distance between each semiconductor device, and the laminated structure of two or more semiconductor devices with an easy configuration can be realized. Moreover, the rewiring substrate has the loading side of a semiconductor device, and can

arrange an electrode pad freely on a rewiring substrate by forming a circuit pattern in this loading side.

[0023] According to invention according to claim 2, a through tube is prepared in INTAPOZA on the background of an electrode pad in which the projection electrode was prepared, the background side of an electrode pad is exposed within a through tube, and a projection electrode is prepared in this field. Moreover, since the height of a projection electrode is higher than the closure height of a semiconductor device, when carrying out the laminating of the semiconductor device of the same structure, the projection electrode of an upper semiconductor device can be connected to the electrode pad of a lower semiconductor device. At this time, the part to which the closure of the semiconductor device of a lower semiconductor device was carried out is held in the space formed with the projection electrode between the rewiring substrate of an upper semiconductor device, and the rewiring substrate of a lower semiconductor device. Therefore, only a projection electrode can prescribe connection of each semiconductor device and the distance between each semiconductor device, and the laminated structure of two or more semiconductor devices with an easy configuration can be realized. Moreover, the rewiring substrate has the loading side of a semiconductor device, and can arrange an electrode pad freely on a rewiring substrate by forming a circuit pattern in this loading side.

[0024] Since according to invention according to claim 3 laminating immobilization of the semiconductor device of further others is carried out at the semiconductor device of a semiconductor device according to claim 1 or 2 and it closes in one, the laminating of the semiconductor device of a laminated structure can be carried out further, and many semiconductor devices can be mounted by the inside of the same volume.

[0025] According to invention according to claim 4, a projection electrode is prepared only in one side of the electrode pad which the semiconductor device was mounted in both sides of a rewiring substrate, and was prepared in both sides of a rewiring substrate. The electrode pad of both sides of a rewiring substrate is electrically connected by the VIA hole. Therefore, the laminating of the semiconductor device which has a projection electrode higher than the closure quantity of the semiconductor device of the side in which the projection electrode is not prepared can be carried out from the side which is not prepared in the projection electrode, and the laminated structure of a semiconductor device can be realized with an easy configuration.

[0026] According to invention according to claim 5, in a semiconductor device according to claim 4, since a projection electrode is more expensive than total of the closure height of the semiconductor device of the both sides of a rewiring substrate, the laminating of the semiconductor devices of the same configuration can be carried out.

[0027] Since according to invention according to claim 6 laminating immobilization of the semiconductor device of further others is carried out at the semiconductor device of a semiconductor device according to claim 4 or 5 and it closes in one, the laminating of the semiconductor device of a laminated structure can be carried out further, and many semiconductor devices can be mounted by the inside of the same volume.

[0028] According to invention according to claim 7, in a semiconductor device according to claim 4 or 5, the semiconductor device of the both sides of a rewiring substrate is connected to an electrode pad by wirebonding. And the connecting location of the wire on the electrode pad of one side has shifted from the connecting location of the wire on the electrode pad of the opposite side. Since the wire is already stretched under the bonding location when performing wirebonding of the semiconductor device of the opposite side after performing wirebonding of the semiconductor device of one side, when the bonding location of the semiconductor device of both sides is the same, a bonding location cannot be supported from the bottom. However, in the semiconductor device by this invention, when performing wirebonding of the semiconductor device of the opposite side after performing wirebonding of the semiconductor device of one side, a bonding location can be supported from the part bottom by which bonding is carried out using a gap of the bonding location of the opposite side, and positive wirebonding can be performed.

[0029] Since it considers as the configuration from which the number of electrodes of the semiconductor device of the top in a laminated structure and the number of electrodes of a lower semiconductor device differ in the semiconductor device which has the laminated structure which carried out the laminating of two or more semiconductor devices indicated by claim 1 thru/or 7, and was connected according to invention according to claim 8, the laminating of the semiconductor devices which have the semiconductor device from which size differs can be carried out.
[0030] Since according to invention according to claim 9 it can carry, supporting the semiconductor device of the opposite side from the bottom after carrying the semiconductor device of one side in case a semiconductor device is carried in both sides of a rewiring substrate, the semiconductor device of both sides can certainly be carried in a rewiring substrate.
[0031] While according to invention according to claim 10 arranging a semiconductor device in the laminating approach of the semiconductor device which carries out the laminating of two or more semiconductor devices by joining a projection electrode and an electrode pad so that a projection electrode may serve as the bottom to the direction of a laminating By imprinting flux on a projection electrode using an imprint head with the fluxing section by which flux is applied only to the arrangement location of a projection electrode, and a corresponding location, flux can be prepared only in a projection electrode. Therefore, it can prevent that the projection electrode and electrode pad which adjoin at the time of the reflow processing carried out in order to join an electrode pad to a projection electrode after FURAKKU spreading short-circuit.
[0032] In the laminating approach of the semiconductor device which carries out the laminating of two or more semiconductor devices by joining a projection electrode and an electrode pad according to invention according to claim 11 By conveying a semiconductor device in the condition that a projection electrode serves as the bottom to the direction of a laminating, immersing a projection electrode in the flux loading section by which only the location corresponding to the arrangement location of a projection electrode was loaded with flux, and arranging flux on a projection electrode Flux can be prepared only in a projection electrode. Therefore, it can prevent that the projection electrode and electrode pad which adjoin at the time of the reflow processing carried out in order to join an electrode pad to a projection electrode after FURAKKU spreading short-circuit.
[0033] Moreover, after usually being manufactured, a semiconductor device is kept so that a projection electrode may be located downward. For this reason, by the laminating approach according to claim 10, the processing which reverses a required semiconductor device becomes unnecessary, and simplification of a flux arrangement process can be attained.
[0034]
[Embodiment of the Invention] Hereafter, the gestalt of the operation in this invention is explained to a detail with reference to a drawing.
[0035] Drawing 3 is the sectional view of the semiconductor device 40 by the 1st example of this invention. The semiconductor device 40 shown in drawing 3 is a semiconductor device of the fan-out mold by which wirebonding connection was made. In drawing 3 , the same sign is given to the same components as the component part shown in drawing 1 , and the explanation is omitted.
[0036] In the semiconductor device 40 shown in drawing 3 , a semiconductor chip 3 is carried in the wiring side side of INTAPOZA 1 which consists of an one side wiring substrate. INTAPOZA 1 is formed from a polyimide tape substrate, a glass epoxy group plate, or an organic substrate (polycarbonate). A semiconductor chip 3 is fixed to INTAPOZA 1 by the DB material 6, and a semiconductor chip 3 and the bonding pad 5 formed on INTAPOZA 1 are electrically connected by carrying out wirebonding with the Au wire 4. A bonding pad 5 is connected to the ball pad 8 by the circuit pattern. The front face of the ball pad 8 is covered with the pewter resist 10 except for the part which forms the pewter ball 7. The pewter ball 7 is formed on the ball pad 8 by the side of the field in which a semiconductor chip 3 is carried.
[0037] The through hole (VIA) 9 where even the ball pad 8 extends is established in the field of the

opposite side of the semiconductor chip 3 loading side of INTAPOZA 1. That is, a through hole 9 is a through tube which penetrates the substrate of INTAPOZA 1 and is prepared. Therefore, the field of the opposite side of the field in which the pewter ball 7 of the ball pad 8 was formed is exposed in a through hole 9. In order to carry out the laminating of the semiconductor device like the after-mentioned and to make connection possible, the magnitude of a through hole 9 is set as magnitude which the ball pad 8 of sufficient area to connect the pewter ball 7 exposes.

[0038] Although the closure of a semiconductor chip 3 and the bonding pad 5 is carried out with closure resin 2, the closure of the ball pad 8 which exposed only the alder dowel-RU loading part by the pewter resist 10 is not carried out. Therefore, the pewter ball 7 is formed on the ball pad 8 exposed by the pewter resist 10. That is, the pewter ball 7 is arranged around a semiconductor chip 3 at the semiconductor chip loading side side of INTAPOZA 1.

[0039] A semiconductor chip 3 is a thin-shape-ized semiconductor chip, and the closure height (height from the ball pad 8 of the part closed with closure resin 2) by closure resin 2 is set up lower than the height (height from the ball pad 8 of the pewter ball 7) of the pewter ball 7. Namely, as it becomes higher than the closure height by closure resin 2, it is set up, and the height of the pewter ball 7 carries out the laminating of the semiconductor device which has the same structure so that it may mention later easily, and has connectable structure. Thus, in order to make the height of closure resin 2 low, when using wirebonding, it is effective to use fluid resin. Moreover, the closure height stabilized lower is realizable by using a vacuum airline printer together.

[0040] Drawing 4 is a semiconductor device by the gestalt of this operation, and is the sectional view showing the example in the case of carrying out flip chip mounting of the semiconductor chip. In drawing 4 , the same sign is given to the same components as the component part shown in drawing 3 , and the explanation is omitted.

[0041] As shown in drawing 4 , it can be made still lower than the case where the closure height by closure resin 2 is shown in drawing 3 , by using flip chip mounting for connection of a semiconductor chip 3. That is, closure height is low pressed down by performing electrical installation of a semiconductor chip 3 and INTAPOZA 1 with the projection electrode 12 which replaced with the Au wire 4 and was formed in the semiconductor chip 3. Au bump or a pewter bump is used as a projection electrode 12.

[0042] Generally between a semiconductor chip 3 and INTAPOZA 1, the under-filling material 11 is poured in, and connection between the projection electrode 12 and a bonding pad 5 is reinforced. By performing impregnation of this under-filling material 11, after forming the pewter ball 7, the under-filling material 11 can be supplied also to the joint of the pewter ball 7 and a ball pad, and connection of the pewter ball 7 can be reinforced. Thereby, the dependability of secondary mounting which mounts a semiconductor device in a substrate can be raised.

[0043] Although the semiconductor device shown in drawing 4 is the so-called exaggerated mold type which closes the semiconductor chip 3 whole with closure resin 2, in flip chip mounting, closure height (closure height turns into height of the top face of a semiconductor chip 3 in this case) can be made lower by excluding the closure by closure resin 2.

[0044] The semiconductor device shown in above-mentioned drawing 3 and above-mentioned drawing 4 can be manufactured in low cost by using INTAPOZA 1 of one side wiring. Moreover, it is not necessary to perform through hole plating to a through hole 9, and can respond also to detailed wiring.

[0045] Drawing 5 is the top view showing the physical relationship of the bonding pad 5 of a semiconductor device and the ball pad 8 using the wirebonding connection shown in drawing 3 . INTAPOZA 1 used for the semiconductor device by the gestalt of this operation can form a circuit pattern also on the field which counters a semiconductor chip 3, as shown in drawing 5 . For this reason, the arrangement relation between a bonding pad 5 and the ball pad 8 can be set up freely, and a bonding pad 5 and the ball pad 8 can be efficiently arranged within a narrow area.

[0046] In addition, although explanation of the semiconductor device by the gestalt of this above-

mentioned operation illustrated and explained the example which connected a semiconductor chip 3 and INTAPOZA 1 by wirebonding and flip chip mounting, INTAPOZA 1 may be used as a tape substrate and a semiconductor chip 3 and INTAPOZA 1 may be connected by TAB (tape auto METEDO bonding) connection.

[0047] Next, the structure which carried out the laminating of two or more semiconductor devices by the 1st example of above-mentioned this invention, and was connected is explained. Drawing 6 is the sectional view showing the example which carried out the two-piece laminating of the semiconductor device which connected the semiconductor chip to INTAPOZA by wirebonding as shown in drawing 3, and was connected. Drawing 7 is the sectional view showing the example which carried out the two-piece laminating of the semiconductor device which connected the semiconductor chip to INTAPOZA by flip chip mounting as shown in drawing 4, and was connected. In drawing 6 and drawing 7, the same sign is given to the same components as the component part shown in drawing 3 and drawing 4, respectively, and the explanation is omitted.

[0048] As shown in drawing 6 and drawing 7, the pewter ball 7 prepared in the upper semiconductor device is connected to the ball pad 8 with which a lower semiconductor device corresponds through the through hole 9 of a lower semiconductor device. Since the height of a pewter ball is higher than the closure height of closure resin 2, spacing between INTAPOZA 1 of an upper semiconductor device and a lower semiconductor device is maintained with the pewter ball 7 more than the closure height of closure resin 2. Therefore, a semiconductor chip 3 is held in the space formed between INTAPOZA 1 of an upper semiconductor device, and INTAPOZA 1 of a lower semiconductor device.

[0049] What is necessary is just to fuse the pewter ball 7 of an upper semiconductor device, after only piling up semiconductor devices, and to connect with the ball pad of a lower semiconductor device in the laminated structure of such a semiconductor device, in order to carry out laminating immobilization of the semiconductor device. Therefore, a laminated structure can be formed by the very easy activity. Moreover, since the pewter ball 7 of an upper semiconductor device is arranged in the through hole 9 formed in INTAPOZA 1 of a lower semiconductor device, positioning of semiconductor devices is performed automatically.

[0050] Drawing 8 is the sectional view showing some semiconductor devices which are the modifications of the semiconductor device by the gestalt of this operation. The same sign is given to the same components as the component part shown in drawing 6 in drawing 8, and the explanation is omitted. In the modification shown in drawing 8, the through hole 9 is formed in the shape of a grinding dovetail. By making a through hole 9 into such a configuration, at the time of positioning of a semiconductor device, the operation to which it shows the pewter ball 7 to a through hole 9 improves, and positioning of semiconductor devices becomes easier. The configuration which is not limited in the shape of a grinding dovetail, and beveled the edge of a through hole 9 is sufficient as the configuration of a through hole 9.

[0051] Moreover, in order to prevent omission of a laminating or the pewter ball by the reflow of the pewter at the time of secondary mounting, it is desirable to make diameter size of a mounting land into 1.5 or less times of the diameter size of opening of a through hole 9. Diameter size of a mounting land and diameter size of opening of a through hole 9 are more preferably made equivalent. Thereby, the area of an up-and-down pewter connection becomes equal, and the fused pewter can be drawn close by one of the two, or can prevent the stress concentration of the joint after mounting. Moreover, as a pewter ball 7 of the semi-conductor used for a laminating, by using a high-melting pewter ball, it can prevent that the pewter ball 7 in a laminated structure remelts the laminating structure to ** secondarily mounted to a mother board, and reliable secondary mounting can be attained.

[0052] The quality of the material of the configuration of the above through holes 9, size, and the pewter ball 7 is explained below, and also it is applicable to an example.

[0053] In addition, in order not to connect the pewter ball 7 to INTAPOZA 1 of a semiconductor device located in the maximum upper case of a laminated structure from the bottom, as shown in drawing 9, there is no need of forming a through hole 9, and it serves as the part cost reduction. Moreover, when

INTAPOZA 1 which formed the through hole 9 is used also for the semiconductor device located in the maximum upper case, electric contact to the semiconductor device by which the laminating was carried out through this through hole 9 can be performed, and the semiconductor device trial of a continuity check etc. can be performed.

[0054] Drawing 10 is the sectional view showing the configuration at the time of making [more] the number of electrodes of the semiconductor device of an upper case than the number of electrodes of the semiconductor device of the lower berth in the laminated structure of the semiconductor device by the gestalt of this operation. In drawing 10 , the same sign is given to the same components as the component part shown in drawing 6 , and the explanation is omitted.

[0055] In drawing 10 , since an upper semiconductor device has many electrodes, it made INTAPOZA 1A of an upper semiconductor device larger than INTAPOZA 1 of a lower semiconductor device, and has prepared ball pad 8A other than the ball pad 8. And ball pad 8A which is not electrically connected with a lower semiconductor device is arranged in the periphery section, and pewter ball 7A linked to this ball pad 8A is formed more greatly than the pewter ball 7. That is, the height of pewter ball 7A is made into the height and EQC to the pewter ball 7 of a lower semiconductor device. Thereby, the electrode of an upper semiconductor device can be electrically connected to other substrates, such as a mother board, without going via the electrode of a lower semiconductor device. Thus, the laminating of the semiconductor device of the different number of electrodes can be carried out by changing the magnitude of a pewter ball. According to the configuration of such a semiconductor device, that of an upper semiconductor device and a lower semiconductor device can be made into the thing of different size, and it becomes possible to carry out the laminating of the semiconductor device of various classes.

[0056] Drawing 11 is the sectional view in the semiconductor device by the gestalt of this operation showing the modification of the ball pad in a through hole. As for ball pad 8B shown in drawing 11 , the field where the pewter ball 7 of an upper semiconductor device is connected is formed in the convex configuration. Thus, by making a ball pad into a convex configuration, a touch area with the pewter ball 7 increases, and reliable connection can be attained.

[0057] In addition, in the laminated structure of the semiconductor device by the above-mentioned example, the semiconductor chip of the semiconductor device by which a laminating is carried out may be a chip of the same kind, and can also be considered as a chip of a different kind. Moreover, although the configuration which carried out the laminating of the two semiconductor devices was explained, the laminating of the three or more semiconductor devices can also be carried out by putting by the same approach.

[0058] Moreover, various modifications in the gestalt of this operation are explained below, and also they are applicable to an example.

[0059] Next, the 2nd example of this invention is explained. Drawing 12 and drawing 13 are the sectional views of the semiconductor device by the 2nd example of this invention. Drawing 12 makes wirebonding connection of the semiconductor chip, and drawing 13 carries out flip chip mounting of the semiconductor chip. In drawing 12 and drawing 13 , the same sign is given to the same components as the component part shown in drawing 3 and drawing 4 . The component part of the semiconductor device by the 2nd example of this invention is fundamentally [as the component part of the semiconductor device by the 1st above-mentioned example] the same, and explains only the difference here.

[0060] In the semiconductor device by the 1st above-mentioned example, the pewter ball 7 is formed in the semiconductor chip loading side, i.e., wiring side, side of INTAPOZA 1. And the closure height of closure resin is set up lower than the height of the pewter ball 7. That is, a semiconductor chip 3 and the pewter ball 7 are carried in the same field side of INTAPOZA 1, and the through hole 9 is established in the field of the opposite side of the semiconductor chip loading side of INTAPOZA 1.

[0061] On the other hand, in the semiconductor device by the 2nd example, the pewter ball 7 is formed in the field of the opposite side of the semiconductor chip loading side of in TAPOZA 1. That is, the

pewter ball 7 is formed to the field of the ball pad 8 exposed in the through hole 9. Therefore, the pewter ball 7 is formed so that it may project in the opposite side of the field in which the semiconductor chip 3 (closure resin 2) was formed.

[0062] In such a configuration, the closure height (height from the front face of the ball pad 8) of closure resin 2 is set up lower than the height (height from the field of the opposite side of the chip component side of INTAPOZA 1) of the pewter ball 7. That is, when the laminating of the semiconductor device by the gestalt of this operation is carried out so that it may mention later since the height of the pewter ball 7 is higher than closure height, the closure part by closure resin 2 is held in the space formed between INTAPOZA of the semiconductor device of a top and the bottom.

[0063] In addition, although explanation of the semiconductor device by the gestalt of this above-mentioned operation illustrated and explained the example which connected a semiconductor chip 3 and INTAPOZA 1 by wirebonding and flip chip mounting, INTAPOZA 1 may be used as a tape substrate and a semiconductor chip 3 and INTAPOZA 1 may be connected by TAB (tape auto METEDO bonding) connection.

[0064] Next, the structure which carried out the laminating of two or more semiconductor devices by the 2nd example of above-mentioned this invention, and was connected is explained. Drawing 14 is the sectional view showing the example which carried out the two-piece laminating of the semiconductor device which connected the semiconductor chip to INTAPOZA by wirebonding as shown in drawing 12 , and was connected. Drawing 15 is the sectional view showing the example which carried out the two-piece laminating of the semiconductor device which connected the semiconductor chip to INTAPOZA by flip chip mounting as shown in drawing 13 , and was connected. In drawing 14 and drawing 15 , the same sign is given to the same components as the component part shown in drawing 12 and drawing 13 , respectively, and the explanation is omitted.

[0065] As shown in drawing 14 and drawing 15 , the pewter ball 7 prepared in the upper semiconductor device is connected to the ball pad 8 with which a lower semiconductor device corresponds through the through hole 9 of a lower semiconductor device. Since the height of the pewter ball 7 is higher than the closure height of closure resin 2, spacing between INTAPOZA 1 of an upper semiconductor device and a lower semiconductor device is maintained with the pewter ball 7 more than the closure height of closure resin 2. Therefore, a semiconductor chip 3 is held in the space formed between INTAPOZA 1 of an upper semiconductor device, and INTAPOZA 1 of a lower semiconductor device.

[0066] What is necessary is just to fuse the pewter ball 7 of an upper semiconductor device, after only piling up semiconductor devices, and to connect with the ball pad of a lower semiconductor device in the laminated structure of such a semiconductor device, in order to carry out laminating immobilization of the semiconductor device. Therefore, a laminated structure can be formed by the very easy activity.

[0067] In addition, in the laminated structure of the semiconductor device by the above-mentioned example, the semiconductor chip of the semiconductor device by which a laminating is carried out may be a chip of the same kind, and can also be considered as a chip of a different kind. Moreover, although the configuration which carried out the laminating of the two semiconductor devices was explained, the laminating of the three or more semiconductor devices can also be carried out by putting one by one by the same approach.

[0068] Next, the 3rd example of this invention is explained. Drawing 16 and drawing 17 are the sectional views showing the semiconductor device by the 3rd example of this invention. In drawing 16 and drawing 17 , the same sign is given to the same components as the component part shown in drawing 3 and drawing 4 , and the explanation is omitted. Fundamental structure is the same as the semiconductor device according [the semiconductor device by the gestalt of this operation] to the 1st above-mentioned example, and difference is that the laminating of the semiconductor chip 3A is carried out, and the resin seal is carried out in one on a semiconductor chip 3.

[0069] In drawing 16 , the laminating of the semiconductor chip 3A smaller than a semiconductor chip 3 is carried out to the semiconductor chip 3 through shock absorbing material 13. Both are connected to

the bonding pad 5 of INTAPOZA 1 by the Au wire 4, and the closure of the semiconductor chips 3 and 3A is carried out in one with closure resin 2. The closure height of closure resin 2 is set up like the semiconductor device by the 1st above-mentioned example lower than the height of pewter ball 7B. Therefore, the semiconductor device by the gestalt of this operation as well as the semiconductor device by the 1st above-mentioned example can carry out the laminating of two or more semiconductor devices, and can be connected.

[0070] The semiconductor device shown in drawing 17 carries out flip chip mounting of the semiconductor chip 3 in the semiconductor device shown in drawing 16 , and other configurations are the same as the semiconductor device shown in drawing 16 .

[0071] Moreover, although illustration is not carried out, TAB connection of the semiconductor device 3 can also be made. Moreover, although the resin seal of the two semiconductor chips is carried out in piles in drawing 16 and drawing 17 , if the closure height of a semiconductor chip can be made lower than the height of pewter ball 7B, it is good also as a configuration which carried out the laminating of the three or more semiconductor devices, carried in INTAPOZA 1 and carried out the resin seal in one.

[0072] Next, the 4th example of this invention is explained. Drawing 18 is the sectional view showing the semiconductor device by the 4th example of this invention. In drawing 18 , the same sign is given to the same components as the component part shown in drawing 12 , and the explanation is omitted. Fundamental structure is the same as the semiconductor device according [the semiconductor device by the gestalt of this operation] to the 2nd above-mentioned example, and difference is that the laminating of the semiconductor chip 3A is carried out, and the resin seal is carried out in one on a semiconductor chip 3.

[0073] In drawing 18 , the laminating of the semiconductor chip 3A smaller than a semiconductor chip 3 is carried out to the semiconductor chip 3 through shock absorbing material 13. Both are connected to the bonding pad 5 of INTAPOZA 1 by the Au wire 4, and the closure of the semiconductor chips 3 and 3A is carried out in one with closure resin 2. The closure height of closure resin 2 is set up like the semiconductor device by the 2nd above-mentioned example lower than the height of pewter ball 7B. Therefore, the semiconductor device by the gestalt of this operation as well as the semiconductor device by the 1st above-mentioned example can carry out the laminating of two or more semiconductor devices, and can be connected.

[0074] Although the semiconductor device shown in drawing 18 carries out wirebonding of the semiconductor chips 3 and 3A, a semiconductor chip 3 can also be mounted in INTAPOZA 1 by flip chip mounting, and may be mounted by TAB connection. Moreover, although the resin seal of the two semiconductor chips is carried out in piles in drawing 18 , if closure height can be made lower than the height of pewter ball 7B, it is good also as a configuration which carried out the laminating of the three or more semiconductor devices, carried in INTAPOZA 1 and carried out the resin seal in one.

[0075] Moreover, although pewter ball 7B higher than the closure height of closure resin 2 is prepared in the semiconductor device shown in drawing 18 , since the pewter ball of the semiconductor device of the bottom is only for connecting with a substrate when carrying out the laminating of two or more semiconductor devices and connecting, there is no need of considering as a large pewter ball.

[0076] Next, the 5th example of this invention is explained. Drawing 19 is the sectional view of the semiconductor device by the 5th example of this invention. In drawing 19 , the same sign is given to the same components as the component part shown in drawing 3 , and the explanation is omitted.

[0077] With the gestalt of this operation, a double-sided wiring substrate is used as INTAPOZA 21. Therefore, a bonding pad 5 and the ball pad 8 are formed in both sides of INTAPOZA 21, a semiconductor chip 3 is carried in both sides of INTAPOZA 21, and a resin seal is carried out. The ball pad 8 or bonding pad 5 of each other prepared in both sides of INTAPOZA 21 is electrically connected by the VIA hole 22. The VIA hole 22 is a hole which penetrates the substrate of INTAPOZA 21, and plating is performed to an inside and it connects the electrode pad of both sides of INTAPOZA electrically. Moreover, pewter ball 7C is prepared in either of the double-sided ball pads 8.

[0078] The height of pewter ball 7C can be carried out to more than the two times of the closure height of closure resin 2, can carry out the laminating of two or more semiconductor devices, and can connect them. That is, when the laminating of the semiconductor device by the gestalt of this operation is carried out and it connects, pewter ball 7C of a semiconductor device located in the bottom is connected to the ball pad 8 of a lower semiconductor device. Between INTABOZA 21 of an upper semiconductor device, and INTAPOZA 21 of a lower semiconductor device, the closure resin 2 of the upper semiconductor chip 3 and the closure resin 2 of the lower semiconductor chip 3 are held. Therefore, it is necessary to carry out the height of pewter ball 7C to more than the two times of the closure height of closure resin 2.

[0079] As it is not necessary to prepare big pewter ball 7C as mentioned above in the semiconductor device located in the bottom here among two or more semiconductor devices by which the laminating was carried out and is shown in drawing 20 , what is necessary is just the pewter ball 7 carried out to more than the height of the closure resin 2 which closes the lower semiconductor chip 3.

[0080] In addition, the semiconductor device by the gestalt of this operation is also good considering a semiconductor chip 3 as well as the above-mentioned example as not wirebonding but flip chip mounting, or TAB connection.

[0081] Drawing 21 (a) and (b) are the mimetic diagrams showing the condition of having carried out the laminating of the modification of the semiconductor device shown in drawing 19 and drawing 20 . In this modification, the height of closure resin 2 is made low except the part which closes a bonding wire (Au wire 4). And it is made for the part to which the closure of the bonding wire of the semiconductor device of a top and the bottom was carried out not to lap by shifting relatively the location of the semiconductor chip 3 of an upper semiconductor device, and the location of the semiconductor chip 2 of a lower semiconductor device. That is, it is the part to which the part which closed the bonding wire becomes the highest in the part of closure resin 2, and by shifting this part of each other and arranging it, spacing of INTAPOZA 21 of an upper semiconductor device and INTAPOZA 21 of a lower semiconductor device can be narrowed, and the height of the whole laminated structure can be made small. In addition, semiconductor devices can also be positioned by fitting the part which closed the bonding wire of one semiconductor device into the part which closed parts other than the bonding wire of the semiconductor device of another side.

[0082] Next, the manufacture approach of the semiconductor device by the 5th example of this invention shown in drawing 19 and drawing 20 is explained.

[0083] Drawing 22 is the mimetic diagram having shown the process which carries a semiconductor chip in INTAPOZA 21. In the 5th example of this invention, a semiconductor chip 3-1 and 3-2 are carried in the both sides of INTAPOZA 21. In case the upper semiconductor chip 3-1 is carried in the field of the opposite side of INTAPOZA 21 after following, for example, carrying the lower semiconductor chip 3-2, INTAPOZA 21 is laid in a fixture 30 and performed. Since the semiconductor chip 3-2 is already carried in the field of the INTAPOZA 21 bottom, the crevice in which a semiconductor chip 3-2 is held is established in a fixture 30. However, when it is going to carry out dice attachment of the semiconductor chip 3-1 as [this] at INTAPOZA 21, INTAPOZA 21 bends according to the load in the case of dice attachment, and there is a possibility that the lower semiconductor chip 3-2 may be contacted and damaged on the base of the crevice of a fixture 30. In order to avoid such a problem, the buffer member 31 is formed in the bottom of a semiconductor chip 3-2, a semiconductor chip -3-2 is supported, and it is made for ******-****** 21 not to bend according to the load in the case of dice attachment of the upper semiconductor chip 3-1. As a buffer member 31, the spring material which has thermal resistance is suitable. As such an ingredient, NBR, silicon system rubber, or fluorine system rubber is mentioned.

[0084] Drawing 23 is the mimetic diagram showing the process at the time of performing wirebonding in the semiconductor device 3-1 of INTAPOZA 21 with which semiconductor chip 3-1 ** 3-2 was carried. In case wirebonding of the semiconductor chip 3-1 of the opposite side is carried out after carrying a semiconductor chip 3-2 in INTAPOZA 21 and performing wirebonding, the load of a wire bonder joins the

connection to INTAPOZA 21 (bonding pad). Since INTAPOZA 21 is formed with a very thin substrate, if WAYABONDINGU is performed where the periphery section of INTAPOZA 21 is supported, INTAPOZA 21 will bend (it will sink in the bottom), and it has a possibility that wirebonding cannot be performed appropriately. In order to avoid such a problem, the bonding wire connection of the upper semiconductor chip 3-1 and the lower semiconductor chip 3-2 is shifted. More specifically, the bonding location of the lower semiconductor chip 3-2 is carried out inside the bonding location of the upper semiconductor chip 3-1. In case wirebonding of the upper semiconductor chip 3-1 is carried out by doing in this way, as shown in drawing 23 , a part for the bonding area of INTAPOZA 21 can be supported on the top face of a fixture 30, and a fixture 30 can receive the load of a wire bonder. Therefore, the problem that INTAPOZA 21 bends and wirebonding cannot be appropriately performed at the time of wirebonding of the upper semiconductor chip 3-1 is avoidable.

[0085] Drawing 24 is the mimetic diagram showing how to avoid the problem by bending of INTAPOZA 21 without using shock absorbing material 31. Drawing 24 (a) is the side elevation of the INTAPOZATO semiconductor chip carried in the fixture, and drawing 24 (b) is the top view seen from the upper part of the half-** chip 3-1. The press member 32 is forced on the part which does not perform wirebonding of INTAPOZA 21, and INTAPOZA 21 will be beforehand sagged to some extent by the approach shown in drawing 24 . Even if the load by the wire bonder is added to INTAPOZA 21 by carrying out wirebonding in the condition that INTAPOZA 21 has tension to some extent where INTAPOZA 21 is sagged, INTAPOZA 21 does not bend any more and can perform wirebonding normally.

[0086] Moreover, it is good also as holding, where INTAPOZA 21 is inserted between the press member 32 and supporter material by preparing supporter material in the part bottom which the press member 32 of INTAPOZA 21 contacts.

[0087] Next, the process which closes the semiconductor device by the 5th example of this invention is explained. Here, two or more semiconductor devices are collectively formed on INTAPOZA 21, and the case where the resin seal of two or more semiconductor devices is carried out is explained. Drawing 25 is the sectional view of the mold metal mold for resin seals, and drawing 26 is the top view showing the interior of the mold metal mold for resin seals.

[0088] The closure process shown in drawing 25 is for carrying out the resin seal of the three semiconductor devices collectively, and the semiconductor chip of six upper and lower sides in all is carried in INTAPOZA 21. INTAPOZA 21 has the magnitude for three semiconductor devices, and it also has the part which extends further in the runner 34 direction of the mold metal mold 33A and 33B. For this reason, in order to introduce resin into both sides of INTAPOZA 21, a runner and the gate must be established in both mold metal mold. Then, as shown in drawing 25 , the gate 34 is established only in punch 33A, opening 21a is prepared in the part of INTAPOZA 21 located near Gates 35A and 35B, and resin is made to be led to both an INTAPOZA 21 top and the bottom. That is, some resin poured in from the INTAPOZA 21 bottom is introduced under INTAPOZA 21 through opening 21a of INTAPOZA 21 within a runner 34. The resin introduced into INTAPOZA a top and the bottom is poured in inside the mold metal mold 33A and 33B at an equal rate through each gates 35A and 33B. Therefore, the resin seal of the semiconductor chip carried in both sides of INTAPOZA 21 by the easy configuration can be carried out to coincidence.

[0089] Moreover, as shown in drawing 25 , in order to carry out the resin seal of two or more semiconductor devices to coincidence, the magnitude of INTAPOZA 21 becomes large and there is a possibility that INTAPOZA 21 may bend in mold metal mold 33A and 33B. In order to prevent this, the substrate bending prevention pin 36 is formed in the mold metal mold 33A and 33B shown in drawing 25 . The substrate bending prevention pin 36 is formed so that it may project from each of the mold metal mold 33A and 33B and INTAPOZA 21 may be contacted. Therefore, INTAPOZA 21 is supported by the substrate bending prevention pin 36, and the bending is prevented. In addition, the part shown with a sign 23 in drawing 26 is a part to which it bends and the prevention pin 36 contacts INTAPOZA 21.

[0090] When especially spacing of a ****** semiconductor chip is narrow, it is desirable to bend in

order to avoid contact to a bonding wire, and to attach a taper to the prevention pin 36. Moreover, it is not necessary to necessarily prepare a bending prevention pin in both punch 33A and female mold 33B, and preparing in female mold 33B can also prevent bending by the weight of INTAPOZA.

[0091] A unnecessary remaining gate is removed by the KATINGU blade and the semiconductor device formed of the above processes is divided into each semiconductor device. Cutting is performed at such a cutting process, boiling the adhesive tape which can exfoliate easily [UV tape etc.], and fixing. However, since the semiconductor chip is carried in both sides of INTAPOZA 21, UV tape cannot stick only to the closure resin section, and cannot be stuck on INTAPOZA 21. Then, the part equivalent to the closure resin of the UV tape 37 is removed, and it is made for the UV tape 37 to stick only to INTAPOZA 21, as shown in drawing 27 . Thereby, INTAPOZA 21 can be fixed on the UV tape 37, and stable cutting can be performed.

[0092] Or punching and laser beam cutting may remove beforehand INTAPOZA 21 other than the part by which the resin seal was carried out, and the configuration stuck on closure resin is sufficient as cutting only closure resin, then the UV tape 37. In this case, a break may be beforehand put into the part which should remove INTAPOZA 21.

[0093] Drawing 28 is the mimetic diagram showing the condition of having carried the semiconductor device by the 5th example of this invention in the substrate. As shown in drawing 28 , a semiconductor device can be carried in the condition of having been stabilized in the substrate 38, by forming shock absorbing material 39 between lower closure resin 2 and the substrates 38, such as a mother board. Shock absorbing material 38 is good also as having the function which buffers the external force which joins a semiconductor device, the function which fixes a semiconductor device to a substrate 38, or the function which emits the heat generated with a semiconductor device to a substrate.

[0094] In addition, without restricting to the semiconductor device by the 5th example of this invention, the shock absorbing material 39 shown in drawing 28 can be applied, if it is the semiconductor device with which the closure of the semiconductor chip was carried out to the INTAPOZA bottom.

[0095] Drawing 29 shows the example which prepared the resist (insulating matter) in the boundary part of the resin seal section. Resist 10A is prepared only in the part which resist 10A does not prepare in the part in which the semiconductor chip of INTAPOZA 21 is carried, but forms the pewter ball 7. Thereby, resist 10A will exist in the joint of mold metal mold, and generating of resin weld flash is controlled by the elasticity of resist 10A. Moreover, it can be made hard to reinforce INTAPOZA 21 by resist 10A, and to bend. Since resist 10A is not prepared in the semiconductor chip loading section, the height of the thickness part semiconductor device of resist 10A can be decreased.

[0096] Although drawing 29 shows the semiconductor device by the 5th example of this invention, it is not restricted to this but, in addition to this, can apply the configuration of resist 10A also to the semiconductor device by the example.

[0097] Drawing 30 shows the example which used the resist for positioning of a semiconductor device. In drawing 30 , resist 10B is not prepared in the part which carries out a resin seal, but when the laminating of the semiconductor device is carried out, it is constituted so that the closure resin 2 of an upper semiconductor device may be positioned by resist 10B of a lower semiconductor device.

[0098] Drawing 30 thru/or drawing 32 are drawings for explaining the laminated structure which combined the semiconductor device by each above-mentioned example. Drawing 31 shows the case where the number of the semiconductor chips contained in a laminated structure is two, drawing 32 shows the case where the number of the semiconductor chips contained in a laminated structure is three, and drawing 33 shows the case where the number of the semiconductor chips contained in a laminated structure is four. In each drawing, the number of a semiconductor chip is displayed on the column of most left-hand side, and the mimetic diagram of a laminated structure is shown in the column whose number is two. The number of INTAPOZA contained in a laminated structure is shown in the 3rd column. The gestalt of an external terminal is shown in the 4th and the 5th column. That is, when it mounts the semiconductor device made into the laminated structure in a substrate, the usable mounting

approach is shown. The 4th column displays O mark, when BGA (ball grid array) is usable, and when it cannot be used, it shows x mark. Moreover, the 5th column displays O mark, when LGA (land grid array) is usable, and when it cannot be used, it shows x mark.

[0099] Moreover, the usable approach is shown in connection of a semiconductor chip at the 6th thru/or the 8th column. That is, in the 6th column, when it can connect by wirebonding, O mark is displayed for a semiconductor chip, and when it cannot connect, x mark is displayed. Moreover, in the 7th column, when flip chip mounting of a semiconductor chip is possible, O mark is displayed, and when flip mounting is impossible, x mark is displayed. Furthermore, in the 8th column, when TAB connection of a semiconductor chip is possible, O mark is displayed, and when not making TAB connection, x mark is displayed.

[0100] In the 9th and the 10th column, the class of semiconductor chip in which combination is possible is specified. That is, in the 9th column, for semiconductor chips of the same kind, when a laminating is possible, O mark is displayed, and when chips of the same kind cannot carry out a laminating, x mark is displayed. In the 10th column, for different-species chips, when a laminating is possible, O mark is displayed, and when the chips of different species cannot carry out a laminating, x mark is displayed.

[0101] Then, the concrete laminating approach which carries out the laminating of the semiconductor device which has the above-mentioned configuration is explained. In addition, in the following explanation, the example which carries out the laminating of the semiconductor device 40 previously explained using drawing 3 is explained.

[0102] Drawing 34 shows the laminating equipment of the semiconductor device used in case the laminating of the semiconductor device 40 is carried out. If the profile of this laminating equipment is carried out, it is constituted by the package supply table 41, the stack head 42, FURAKKU feed zone 43A, imprint head 44A, and camera unit 45 grade.

[0103] The package supply table 41 is a table on which the semiconductor device 40 manufactured by the above mentioned manufacture approach is laid temporarily. In this example, each semiconductor device 40 is laid on the package supply table 41 so that the pewter ball 7 may serve as a top face.

[0104] In addition, the manufactured semiconductor device 40 is conveyed after even this laminating equipment has been contained by the tray for conveyance. Under the present circumstances, for the reasons of protection of the pewter ball 7 etc., a semiconductor device 40 turns the pewter ball 7 down, and is contained by the tray for conveyance. Therefore, the semiconductor device 40 which was picked out from the tray for conveyance in the case of this example is laid in the package supply table 41, after the upper and lower sides are reversed.

[0105] The stack head 42 is considered as the configuration movable in three dimensions by the migration equipments (for example, robot etc.) which are not illustrated. Moreover, the adsorption head section 47 connected to the aspirator is formed in the point, and it considers as the configuration which can be held by attracting a semiconductor device 40.

[0106] FURAKKU feed zone 43A applies FURAKKU 50 to imprint head 44A mentioned later. This flux feed zone 43A is made into the shape of a cylindrical shape, and that top face is considered as the configuration with high flatness. After the top face of this FURAKKU feed zone 43A is loaded with flux 50, let it be predetermined thickness using a squeegee 48. The thickness of the flux 50 at this time can be set as the thickness of arbitration by adjusting the path clearance between a squeegee 48 and FURAKKU feed zone 43A.

[0107] Imprint head 44A is considered as the configuration movable in three dimensions by the migration equipments (for example, robot etc.) which are not illustrated. And by being pushed against the flux 50 by which the point (lower limit section in drawing) of imprint head 44A was arranged in FURAKKU feed zone 43A with this migration, flux 50 is constituted so that it may move to imprint head 44A from FURAKKU feed zone 43A.

[0108] The camera unit 45 is considered as the configuration with the up camera 51 which picturizes the upper part, and the lower camera 52 which picturizes the lower part. In case this camera unit 45

carries out the laminating of two or more semiconductor devices 40 so that it may mention later, it is used for positioning each semiconductor device 40.

[0109] In addition, this example shall explain the example which carries out the laminating of the two semiconductor devices. Moreover, when a laminating is carried out, sign 40A shall show the semiconductor device located in the lower part, and sign 40B shall show the semiconductor device located in the upper part. Furthermore, a sign 40 shall be used when a semiconductor device is shown irrespective of the upper part and the lower part.

[0110] Since the camera unit 45 is considered as the configuration which formed the up camera 51 and the lower camera 52 in one, when a laminating is carried out, it can picturize to coincidence semiconductor device 40A located in the lower part, and semiconductor device 40B located in the upper part, so that it may be illustrated. Therefore, compared with the configuration which has formed only one camera, it becomes unnecessary to be able to reverse a camera and the increase in efficiency of positioning processing can be attained.

[0111] Next, the laminating approach of the semiconductor devices 40A and 40B performed using the laminating equipment considered as the above-mentioned configuration is explained.

[0112] In order to carry out the laminating of the semiconductor devices 40A and 40B, carrier stage 46A is equipped with semiconductor device 40A first located in the bottom. Carrier stage 46A becomes a pedestal at the time of carrying out the laminating of each semiconductor devices 40A and 40B. Drawing 35 shows the condition of having equipped carrier stage 46A with semiconductor device 40A.

[0113] As shown in this drawing, wearing slot 49A for positioning semiconductor device 40A is formed in carrier stage 46A. The stack head 42 conveys semiconductor device 40A located in the bottom from the package supply table 41, and equips with it in wearing slot 49A of carrier stage 46A.

[0114] As described above, each semiconductor device 40 is laid in the package supply table 41 so that the pewter ball 7 may be located in the upper part. Moreover, the stack head 42 performs conveyance processing by adsorbing the front face of the closure resin 2 of a semiconductor device 40. Therefore, in the condition that carrier stage 46A was equipped, semiconductor device 40A is the posture in which the pewter ball 7 is located in the upper part.

[0115] Processing which applies flux 50 to imprint head 44A is carried out after conveyance processing of this semiconductor device 40A (it is also possible to carry out to conveyance processing and coincidence). In order to apply flux 50 to imprint head 44A, as shown in drawing 36 , imprint head 44A is forced on flux feed zone 43A applied to flux 50. As described above, flux 50 is arranged in flux feed zone 43A by predetermined thickness. Therefore, flux 50 adheres to imprint head 44A by forcing imprint head 44A on flux feed zone 43A.

[0116] Thus, imprint head 44A in which flux 50 was arranged moves to carrier stage 46A. Then, imprint head 44A is forced on semiconductor device 40A with which carrier stage 46A is equipped. As described above, carrier stage 46A is equipped with semiconductor device 40A with the posture in which the pewter ball 7 is located in the upper part. Therefore, the flux 50 currently arranged in imprint head 44A is imprinted by the pewter ball 7 by forcing imprint head 44A on semiconductor device 40A.

[0117] Under the present circumstances, the flux 50 arranged in imprint head 44A is imprinted by only the pewter ball 7, and it consists of this examples so that it may not adhere to other parts which constitute semiconductor device 40A of closure resin 2 grade. Hereafter, this reason is explained.

[0118] Drawing 38 is drawing expanding and showing the base (field forced on flux feed zone 43A and semiconductor device 40A) of imprint head 44A. As shown in this drawing, the crevice 53 is formed in the base of imprint head 44A, and fluxing section 54A which this projected to the crevice 53 relatively is formed.

[0119] The arrangement location of this fluxing section 54A is constituted so that it may correspond with the arrangement location of the pewter ball 7 of semiconductor device 40A. Moreover, the arrangement location of a crevice 53 is constituted so that abbreviation correspondence may be carried out with the arrangement location of the closure resin 2 of semiconductor device 40A. Therefore, when

imprint head 44A considered as the above-mentioned configuration is forced on flux feed zone 43A, flux 50 adheres only to fluxing section 54A, and does not adhere to a crevice 53.

[0120] When this forces on semiconductor device 40A imprint head 44A in which flux 50 was arranged, flux 50 is imprinted by only the pewter ball 7 as shown in drawing 40 . Moreover, when imprint head 44A is forced on semiconductor device 40A, since closure resin 2 will be in the condition of countering with the crevice 53 of imprint head 44A, the top face and crevice 53 of closure resin 2 will be in the condition of having estranged greatly. For this reason, it can prevent certainly that flux 50 is accidentally applied to closure resin 2.

[0121] After FURAKKU spreading, reflow processing which joins the ball pad 8 of semiconductor device 40B to the pewter ball 7 of the laminating processing which carries out the laminating of the semiconductor devices 40A and 40B, and semiconductor device 40A is performed so that it may mention later. Under the present circumstances, when flux 50 exists in addition to the arrangement location of the pewter ball 7, there is a possibility that the conductive metals (pewter etc.) which constitute flux 50 may fuse, and a short circuit may arise between adjoining pewter balls or between ball pads.

[0122] However, by considering as the configuration flux 50 is imprinted by only whose pewter ball 7 like this example, it can prevent connecting too hastily between adjoining pewter balls and between adjoining ball pads, and improvement in dependability can be aimed at.

[0123] In order to prevent connecting too hastily between adjoining pewter balls or between adjoining ball pads on the other hand, it is necessary to imprint the flux 50 of optimum dose on the pewter ball 7. This is because there is a possibility that a short circuit may occur between the pewter balls which adjoin by the excessive flux 50, or between adjoining ball pads when the flux 50 more than an initial complement is imprinted by the pewter ball 7.

[0124] Moreover, it is because there is a possibility of an oxide film being formed in the front face of the pewter ball 7, and generating a faulty connection between the pewter ball 7 and the ball pad 8 at the time of a laminating when there are few amounts of the flux 50 imprinted (there is a function to prevent scaling of the pewter ball 7 at the time of heating in flux 50).

[0125] It is possible to select suitably formation of Lux spreading section 54A prepared in imprint head 44A other than the approach of controlling the thickness of the flux 50 applied to flux feed zone 43A as an approach of imprinting the flux 50 of optimum dose on the pewter ball 7. This is explained using drawing 39 .

[0126] Drawing 39 (A) expands and shows fluxing section 54of imprint head 44A shown in drawing 38 A. As shown in this drawing, in fluxing section 54A made into the flat-surface configuration, there are few amounts of the flux 50 imprinted from flux feed zone 43A.

[0127] However, the amount of the flux 50 adhering to the fluxing sections 54A-54C is controllable by an inclined plane's constituting fluxing section 54B, as shown in drawing 39 (B), and constituting fluxing section 54B by the concave spherical surface, as shown in drawing 39 (B). This becomes possible to imprint the flux 50 of optimum dose on the pewter ball 7.

[0128] After the processing which imprints flux 50 on the pewter ball 7 as mentioned above is completed, while the stack head 42 moves onto the package supply table 41 again, it lower-**, and as shown in drawing 41 , semiconductor device 40B which carries out a laminating on semiconductor device 40A is adsorbed. With actuation of this stack head 42, the camera knitting 45 moves to the upper part of the carrier stage 46. Under the present circumstances, the lower camera 52 moves the camera unit 45 to semiconductor device 40A with which carrier stage 46A was equipped, and the location which counters.

[0129] On the other hand, the stack head 42 which adsorbed semiconductor device 40B conveys semiconductor device 40B to the up camera 51 of the camera unit 45, and the location which counters. This becomes the configuration that insert the camera unit 45 in the middle, semiconductor device 40A is located in the lower part, and semiconductor device 40B is located in the upper part, as shown in drawing 42 . And the up camera 51 performs location recognition of the ball pad 8 of semiconductor

device 40B. and the lower camera 52 performs location recognition of the pewter ball 7 of semiconductor device 40A. Thereby, location recognition of each semiconductor devices 40A and 40B is performed.

[0130] The laminating of the semiconductor device 40B is carried out on semiconductor device 40A so that the stack head 42 of the location of the ball pad 8 of semiconductor device 40B and the pewter ball 7 of semiconductor device 40A may correspond based on this recognition result continuously, if location recognition processing of each semiconductor devices 40A and 40B is performed as mentioned above. Thereby, as shown in drawing 44 , semiconductor devices 40A and 40B will be in the condition that the laminating was carried out. Under the present circumstances, as mentioned above, since flux 50 is the configuration imprinted by only the upper part of the pewter ball 7, flux 50 does not exist between the closure resin 2 of semiconductor device 40A located in the lower part, and INTAPOZA 1 of semiconductor device 40B located in the upper part.

[0131] The condition which shows in drawing 44 is the configuration by which it was tacking carried out by the flux 50 to which each semiconductor devices 40A and 40B intervene between the pewter ball 7 of semiconductor device 40A located in the lower part, and the ball pad 8 of semiconductor device 40B located in the upper part. For this reason, where a laminating is carried out, semiconductor devices 40A and 40B put carrier stage 46A into a reflow furnace, and join the pewter ball 7 by solder to the ball pad 8. Thereby, it is fixed and each semiconductor devices 40A and 40B serve as a configuration by which the laminating was carried out completely.

[0132] In addition, although this example explained the configuration which carries out the laminating of the two semiconductor devices 40A and 40B, when carrying out the laminating of the three or more semiconductor devices 40, the laminated structure of the number of arbitration can be realized by repeating and carrying out the above-mentioned processing.

[0133] Drawing 45 - drawing 48 are drawings for explaining the modification of the above-mentioned laminating approach.

[0134] In case the modification shown in drawing 45 imprints flux 50 (not shown to drawing 45) to the pewter ball 7, it is made to perform plastic surgery processing of the pewter ball 7 to coincidence. That is, there is variation in the magnitude of the pewter ball 7, and although the pewter ball 7 of a large diameter is joined when this variation is large, and the laminating of the semiconductor devices 40A and 40B is carried out, the pewter ball 7 of a small diameter has a possibility that junction may be impossible.

[0135] For this reason, in this modification, it is characterized by considering as the configuration which performs leveling of the pewter ball 7 using imprint head 44D. For this reason, in this modification, hard stainless steel material is used as the quality of the material of imprint head 44D. And imprint head 44D is made to lower-**, maintaining a level condition at the time of imprint processing of flux 50, as shown in drawing 45 (A) and (B), and the pewter ball 7 is pressurized.

[0136] Thereby, as shown in drawing 45 (C), flat falsework 7A is formed in the top face of the pewter ball 7. Thus, by performing leveling of the pewter ball 7 using imprint head 44D, the height of the pewter ball 7 can be equalized and generating of the faulty connection at the time of a laminating can be controlled. Moreover, since flat falsework 7A is formed in the upper limit section of the pewter ball 7, the imprint nature of flux 50 also improves. Furthermore, the above-mentioned effectiveness can be realized, without increasing the process of laminating processing, in order to perform leveling processing to imprint processing and coincidence of flux 50.

[0137] In case the modification shown in drawing 46 carries out the laminating of the semiconductor devices 40A and 40B, it is made to perform positioning of each semiconductor devices 40A and 40B using the positioning fixture 55. The positioning fixture 55 is constituted by the positioning members 55A-55C.

[0138] When each of these positioning members 55A-55C are accumulated, they are considered as the configuration with which a mutual location is positioned in a predetermined location by the gage pin and tooling holes which are not illustrated. Tooling-holes 59A contained where positioning member 55A

positions semiconductor device 40A and semiconductor device 40A is positioned inside is formed.
[0139] Moreover, tooling-holes 59B contained where positioning member 55B positions semiconductor device 40B and semiconductor device 40B is positioned inside is formed. Furthermore, positioning member 55C is arranged in the topmost part, and the opening 56 which fluxing section 54A of imprint head 44E inserts is formed.
[0140] Therefore, by equipping the positioning fixture 55 with semiconductor devices 40A and 40B, positioning processing of each semiconductor devices 40A and 40B can be performed, and it can position easily. Therefore, when semiconductor device 40A and 40B shift, it can prevent that flux 50 adheres in addition to pewter ball 7.
[0141] Moreover, the modification shown in drawing 47 fixes the positioning fixture 55 explained using drawing 46 by the clip member 57, and is characterized by performing reflow processing in this condition. It is positioned by high degree of accuracy by using the positioning fixture 55 by considering as this configuration, and reflow processing of each semiconductor devices 40A and 40B can be carried out, maintaining the condition of having been tacking carried out by flux 50. Thereby, even if flux 50 will be in a melting condition with heating, the laminating of each semiconductor devices 40A and 40B can be carried out with a high location precision. In addition, the approach of the overheating processing which joins the ball pad 8 to the pewter ball 7 is not limited to reflow processing, and can also use the block heater method, laser, or the hot-air method.
[0142] Then, other laminating approaches which carry out the laminating of the semiconductor devices 40A and 40B are explained.
[0143] Drawing 48 shows the laminating equipment of the semiconductor device used in case the laminating of the semiconductor device 40 is carried out in this example. In addition, in drawing 48 , about the same configuration as the configuration shown in drawing 34 explained previously, the same sign is attached and the explanation is omitted.
[0144] If the profile of the laminating equipment used for the laminating approach of this example is carried out, it is constituted by the package supply table 41, the stack head 42, FURAKKU feed zone 43B, and camera unit 45 grade. Therefore, the configuration is simplified compared with the laminating equipment shown in drawing 34 which needed imprint head 44A.
[0145] The package supply table 41 is the same configuration as what was shown in drawing 34 . However, in this example, each semiconductor device 40 is laid on the package supply table 41 so that the pewter ball 7 may serve as an inferior surface of tongue. As described above, the manufactured semiconductor device 40 turns the pewter ball 7 down, and is contained by the tray for conveyance.
[0146] Therefore, in the case of this example, since the semiconductor device 40 picked out from the tray for conveyance can be laid in the package supply table 41 with a posture as it is, processing which moves a semiconductor device 40 from the tray for conveyance to the supply table 41 can be performed easily. Moreover, when the stack head 42 adsorbs the semiconductor device 40 on the package supply table 41, semiconductor device 40B will be in the condition that the pewter ball 7 was located in the lower part.
[0147] FURAKKU feed zone 43B used by this example is considered as the configuration which applies direct FURAKKU 50 to the pewter ball 7 of semiconductor device 40B. This flux feed zone 43B is made into the shape of a cylindrical shape, and the flux loading slot 58 is formed in that top face. The flux loading slot 58 has the rectangle frame-like configuration, where plane view is carried out. Moreover, this flux loading slot 58 is constituted so that it may correspond to the arrangement location of semiconductor device 40B, and in case flux 50 is imprinted on the pewter ball 7 so that it may mention later, the pewter ball 7 is inserted into the flux loading slot 58.
[0148] In this example, flux 50 is arranged only in the flux loading slot 58. In order to load with flux 50 into the flux loading slot 58, after arranging flux 50 in the top face of FURAKKU feed zone 43A, as shown in drawing 50 , it inserts into the flux loading slot 58 using a squeegee 48. In addition, the thickness of flux 50 can be set as the thickness of arbitration by adjusting the depth of the flux loading

slot 58.

[0149] Next, the laminating approach of the semiconductor devices 40A and 40B performed using the laminating equipment considered as the above-mentioned configuration is explained.

[0150] In order to carry out the laminating of the semiconductor devices 40A and 40B, carrier stage 46B is equipped with semiconductor device 40A first located in the bottom. Drawing 49 shows the condition of having equipped carrier stage 46B with semiconductor device 40A. As shown in this drawing, wearing slot 49B for positioning semiconductor device 40A is formed in carrier stage 46A. The stack head 42 conveys semiconductor device 40A from the package supply table 41, and equips with it in wearing slot 49B of carrier stage 46B.

[0151] As described above, each semiconductor device 40 is laid in the package supply table 41 so that the pewter ball 7 may be located in the lower part. Moreover, the stack head 42 performs conveyance processing by adsorbing INTAPOZA 1 of a semiconductor device 40. Therefore, in the condition that carrier stage 46B was equipped, semiconductor device 40A is the posture in which the pewter ball 7 is located in the lower part.

[0152] Processing which loads with flux 50 to flux feed zone 43B using 48 at the time of skiing after conveyance processing of this semiconductor device 40A (it is also possible to carry out to conveyance processing and coincidence) as described above is carried out (refer to drawing 50). After the processing which loads with flux 50 to flux feed zone 43B is completed, while the stack head 42 moves onto the package supply table 41 again, it lower-**, and as shown in drawing 51, semiconductor device 40B which carries out a laminating on semiconductor device 40A is adsorbed.

[0153] To the upper part of the flux loading slot 58 on flux feed zone 43B, semiconductor device 40B is conveyed and the stud head 42 lower-** it continuously. In case semiconductor device 40B is conveyed by the stud head 42, it is the posture in which the pewter ball 7 is located in the lower part. Therefore, when the stud head 42 lower-**, as shown in drawing 52 , it is immersed in the flux 50 in the flux restoration slot 58 by the pewter ball 7. Thereby, flux 50 is imprinted by the pewter ball 7.

[0154] Under the present circumstances, flux 50 is imprinted by only the pewter ball 7 and other parts which constitute semiconductor device 40A of closure resin 2 grade do not adhere to it. That is, flux feed zone 43B has the composition that only the flux restoration slot 58 was loaded with flux 50, and the flux restoration slot 58 has composition corresponding to the arrangement location of the pewter ball 7. Furthermore, in case the flux restoration slot 58 is loaded with flux 50, it constitutes so that flux 50 may not adhere to any parts other than flux restoration slot 58 of flux feed zone 43B.

[0155] Thereby, flux 50 is imprinted by only the pewter ball 7 when the pewter ball 7 of semiconductor device 40B is made immersed in the flux 50 in the flux restoration slot 58. Therefore, it can prevent connecting too hastily between adjoining pewter balls and between adjoining ball pads also by this example, and improvement in the dependability after a laminating can be aimed at.

[0156] As for the stack head 42, termination of the processing which imprints flux 50 on the pewter ball 7 as mentioned above conveys semiconductor device 40B to the upper part (location which specifically counters with semiconductor device 40A) of carrier stage 46B. With this, the camera knitting 45 also moves to the upper part of the carrier stage 46. This becomes the configuration that insert the camera unit 45 in the middle, semiconductor device 40A is located in the lower part, and semiconductor device 40B is located in the upper part, as shown in drawing 53 . And the upper camera 51 arranged in the camera unit 45 performs location recognition of the ball pad 8 of semiconductor device 40B, the lower camera 52 performs location recognition of the pewter ball 7 of semiconductor device 40A, and, thereby, location recognition of each semiconductor devices 40A and 40B is performed.

[0157] When location recognition processing of each semiconductor devices 40A and 40B is performed as mentioned above, as the stack head 42 is continuously shown in drawing 54 based on this recognition result, the laminating of the semiconductor device 40B is carried out on semiconductor device 40A so that the location of the ball pad 8 of semiconductor device 40B and the pewter ball 7 of semiconductor device 40A may be in agreement.

[0158] Thereby, as shown in drawing 55 , semiconductor devices 40A and 40B will be in the condition that the laminating was carried out. Under the present circumstances, as mentioned above, since flux 50 is the configuration imprinted by only the upper part of the pewter ball 7, flux 50 does not exist between the closure resin 2 of semiconductor device 40B located in the upper part, and INTAPOZA 1 of semiconductor device 40A located in the lower part.

[0159] The condition which shows in drawing 55 is the configuration of having been tacking carried out of semiconductor device 40A and the semiconductor device 40B by flux 50. For this reason, where a laminating is carried out, semiconductor devices 40A and 40B put carrier stage 46B into a reflow furnace, and join the pewter ball 7 by solder to the ball pad 8. Thereby, it is fixed and each semiconductor devices 40A and 40B serve as a configuration by which the laminating was carried out completely.

[0160] In addition, also in this example, when carrying out the laminating of the three or more semiconductor devices 40, thereby, the laminated structure of the number of arbitration can be realized that what is necessary is just to repeat and carry out the above-mentioned processing.

[0161]

[Effect of the Invention] As explained above, according to invention according to claim 1, a through tube is prepared in INTAPOZA on the background of an electrode pad in which the projection electrode was prepared, and the background side (field of a projection electrode and the opposite side) of an electrode pad is exposed within a through tube. Moreover, since the height of a projection electrode is higher than the closure height of a semiconductor device, when carrying out the laminating of the semiconductor device of the same structure, the projection electrode of an upper semiconductor device can be connected to the electrode pad in the through tube of a lower semiconductor device. At this time, the part to which the closure of the semiconductor device of an upper semiconductor device was carried out is held in the space formed with the projection electrode between the rewiring substrate of an upper semiconductor device, and the rewiring substrate of a lower semiconductor device.

[0162] Therefore, only a projection electrode can prescribe connection of each semiconductor device and the distance between each semiconductor device, and the laminated structure of two or more semiconductor devices with an easy configuration can be realized. Moreover, the rewiring substrate has the loading side of a semiconductor device, and can arrange an electrode pad freely on a rewiring substrate by forming a circuit pattern in this loading side.

[0163] According to invention according to claim 2, a through tube is prepared in INTAPOZA on the background of an electrode pad in which the projection electrode was prepared, the background side of an electrode pad is exposed within a through tube, and a projection electrode is prepared in this field. Moreover, since the height of a projection electrode is higher than the closure height of a semiconductor device, when carrying out the laminating of the semiconductor device of the same structure, the projection electrode of an upper semiconductor device can be connected to the electrode pad of a lower semiconductor device. At this time, the part to which the closure of the semiconductor device of a lower semiconductor device was carried out is held in the space formed with the projection electrode between the rewiring substrate of an upper semiconductor device, and the rewiring substrate of a lower semiconductor device.

[0164] Therefore, only a projection electrode can prescribe connection of each semiconductor device and the distance between each semiconductor device, and the laminated structure of two or more semiconductor devices with an easy configuration can be realized. Moreover, the rewiring substrate has the loading side of a semiconductor device, and can arrange an electrode pad freely on a rewiring substrate by forming a circuit pattern in this loading side.

[0165] Since according to invention according to claim 3 laminating immobilization of the semiconductor device of further others is carried out at the semiconductor device of a semiconductor device according to claim 1 or 2 and it closes in one, the laminating of the semiconductor device of a laminated structure can be carried out further, and many semiconductor devices can be mounted by the inside of the same

volume.

[0166] According to invention according to claim 4, a projection electrode is prepared only in one side of the electrode pad which the semiconductor device was mounted in both sides of a rewiring substrate, and was prepared in both sides of a rewiring substrate. The electrode pad of both sides of a rewiring substrate is electrically connected by the VIA hole. Therefore, the laminating of the semiconductor device which has a projection electrode higher than the closure quantity of the semiconductor device of the side in which the projection electrode is not prepared can be carried out from the side which is not prepared in the projection electrode, and the laminated structure of a semiconductor device can be realized with an easy configuration.

[0167] According to invention according to claim 5, in a semiconductor device according to claim 4, since a projection electrode is more expensive than total of the closure height of the semiconductor device of the both sides of a rewiring substrate, the laminating of the semiconductor devices of the same configuration can be carried out.

[0168] Since according to invention according to claim 6 laminating immobilization of the semiconductor device of further others is carried out at the semiconductor device of a semiconductor device according to claim 4 or 5 and it closes in one, the laminating of the semiconductor device of a laminated structure can be carried out further, and many semiconductor devices can be mounted by the inside of the same volume.

[0169] According to invention according to claim 7, in a semiconductor device according to claim 4 or 5, the semiconductor device of the both sides of a rewiring substrate is connected to an electrode pad by wirebonding. And the connecting location of the wire on the electrode pad of one side has shifted from the connecting location of the wire on the electrode pad of the opposite side.

[0170] Since the wire is already stretched under the bonding location when performing wirebonding of the semiconductor device of the opposite side after performing wirebonding of the semiconductor device of one side, when the bonding location of the semiconductor device of both sides is the same, a bonding location cannot be supported from the bottom.

[0171] However, in the semiconductor device by this invention, when performing wirebonding of the semiconductor device of the opposite side after performing wirebonding of the semiconductor device of one side, a bonding location can be supported from the part bottom by which bonding is carried out using a gap of the bonding location of the opposite side, and positive wirebonding can be performed.

[0172] Since it considers as the configuration from which the number of electrodes of the semiconductor device of the top in a laminated structure and the number of electrodes of a lower semiconductor device differ in the semiconductor device which has the laminated structure which carried out the laminating of two or more semiconductor devices indicated by claim 1 thru/or 7, and was connected according to invention according to claim 8, the laminating of the semiconductor devices which have the semiconductor device from which size differs can be carried out.

[0173] Since according to invention according to claim 9 it can carry, supporting the semiconductor device of the opposite side from the bottom after carrying the semiconductor device of one side in case a semiconductor device is carried in both sides of a rewiring substrate, the semiconductor device of both sides can certainly be carried in a rewiring substrate.

[0174] According to invention claim 10 and given in 11, it can prevent that the projection electrode and electrode pad which adjoin at the time of the reflow processing carried out in order to be able to prepare flux only in a projection electrode, to accumulate and to join an electrode pad to a projection electrode after FURAKKU spreading short-circuit.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the sectional view of the semiconductor device of the fan-out mold by the conventional wirebonding.

[Drawing 2] It is the sectional view of the semiconductor device by the conventional flip chip mounting.

[Drawing 3] It is the sectional view of an example of the semiconductor device by the 1st example of this invention.

[Drawing 4] It is the sectional view of the modification of the semiconductor device by the 1st example of this invention.

[Drawing 5] It is the top view of INTAPOZA of the semiconductor device by the 1st example of this invention.

[Drawing 6] It is the sectional view showing the structure which carried out the laminating of the semiconductor device shown in drawing 3 .

[Drawing 7] It is the sectional view showing the structure which carried out the laminating of the semiconductor device shown in drawing 4 .

[Drawing 8] It is the sectional view showing the modification of the semiconductor device shown in drawing 4 .

[Drawing 9] It is the sectional view showing an example of the laminated structure of the semiconductor device shown in drawing 4 .

[Drawing 10] It is the sectional view showing the modification of the semiconductor device shown in drawing 4 .

[Drawing 11] It is the sectional view showing the modification of a ball pad.

[Drawing 12] It is the sectional view of an example of the semiconductor device by the 2nd example of this invention.

[Drawing 13] It is the sectional view of the modification of the semiconductor device by the 2nd example of this invention.

[Drawing 14] It is the sectional view of the structure which carried out the laminating of the semiconductor device shown in drawing 12 .

[Drawing 15] It is the sectional view of the structure which carried out the laminating of the semiconductor device shown in drawing 13 .

[Drawing 16] It is the sectional view of an example of the semiconductor device by the 3rd example of this invention.

[Drawing 17] It is the sectional view of the modification of the semiconductor device by the 3rd example of this invention.

[Drawing 18] It is the sectional view of the semiconductor device by the 4th example of this invention.

[Drawing 19] It is the sectional view of an example of the semiconductor device by the 5th example of this invention.

[Drawing 20] It is the sectional view of the modification of the semiconductor device by the 5th example of this invention.

[Drawing 21] It is the mimetic diagram showing the structure which carried out the laminating of the

modification of the semiconductor device shown in drawing 19 and drawing 20.
[Drawing 22] It is the mimetic diagram showing the chip loading process of the semiconductor device by the 5th example of this invention.
[Drawing 23] It is the mimetic diagram showing the wirebonding process of the semiconductor device by the 5th example of this invention.
[Drawing 24] It is the mimetic diagram showing the wirebonding process of the semiconductor device by the 5th example of this invention.
[Drawing 25] It is the mimetic diagram showing the resin seal process of the semiconductor device by the 5th example of this invention.
[Drawing 26] It is the mimetic diagram showing the resin seal process of the semiconductor device by the 5th example of this invention.
[Drawing 27] It is the mimetic diagram showing the process which cuts down each semiconductor device.
[Drawing 28] It is the mimetic diagram showing the condition of having carried the semiconductor device by the 5th example of this invention in the substrate.
[Drawing 29] It is the mimetic diagram showing the example which reinforces INTAPOZA by the resist.
[Drawing 30] It is the mimetic diagram showing the example which positions a semiconductor device by the resist.
[Drawing 31] It is drawing for explaining the laminated structure which combined the semiconductor device by this invention example.
[Drawing 32] It is drawing for explaining the laminated structure which combined the semiconductor device by this invention example.
[Drawing 33] It is drawing for explaining the laminated structure which combined the semiconductor device by this invention example.
[Drawing 34] It is the important section block diagram showing the laminating equipment used for the laminating approach of the semiconductor device by this invention example.
[Drawing 35] It is drawing showing the semiconductor device with which the carrier stage was equipped.
[Drawing 36] It is drawing for explaining how applying flux to an imprint head.
[Drawing 37] It is drawing for explaining how imprinting flux on a pewter ball using an imprint head.
[Drawing 38] It is a perspective view for explaining the detail of an imprint head.
[Drawing 39] It is drawing for explaining the structure of various imprint heads.
[Drawing 40] It is drawing showing the condition that flux was arranged on a pewter ball.
[Drawing 41] It is drawing showing the condition of adsorbing the semiconductor device on a package supply table by the stack head.
[Drawing 42] It is drawing showing the condition of performing location recognition processing of each semiconductor device using the camera unit.
[Drawing 43] It is drawing showing the condition of carrying out the laminating of the semiconductor device.
[Drawing 44] It is drawing showing the semiconductor device by which the laminating was carried out.
[Drawing 45] It is drawing for explaining how to operate a pewter ball orthopedically by the imprint head.
[Drawing 46] It is drawing for explaining how raising the location precision of the semiconductor device by which the laminating was carried out using the positioning fixture.
[Drawing 47] It is drawing for explaining how to perform reflow processing where a positioning fixture is fixed by the clip member.
[Drawing 48] It is the important section block diagram showing the laminating equipment used for the laminating approach of the semiconductor device by this invention example.
[Drawing 49] It is drawing showing the semiconductor device with which the carrier stage was equipped.
[Drawing 50] It is drawing for explaining how to load the FURAKKU loading section of a flux feed zone with flux.
[Drawing 51] It is drawing showing the condition of adsorbing the semiconductor device on a package

supply table by the stack head.
[Drawing 52] It is drawing for explaining how arranging flux in the pewter ball of a semiconductor device.
[Drawing 53] It is drawing showing the condition of performing location recognition processing of each semiconductor device using the camera unit.
[Drawing 54] It is drawing showing the condition of carrying out the laminating of the semiconductor device.
[Drawing 55] It is drawing showing the semiconductor device by which the laminating was carried out.
[Description of Notations]
1, 1A, 21 INTAPOZA
2 Closure Resin
3, 3A, 3-1, 3-2 Semiconductor chip
4 Au Wire
5 Bonding Pad
6 DB Material
7, 7A, 7B, 7C Pewter ball
8 8B Ball pad
9 Through Hole
10 Solder Resist
10A, 10B Resist
11 Under-filling Material
12 Projection Electrode
21a Opening
22 VIA Hole
24 UV Tape
13 39 Shock absorbing material
30 Fixture
31 Buffer Member
32 Press Member
33A, 33B Mold metal mold
34 Runner
35A, 35B Gate
36 Bending Prevention Pin
37 UV Tape
38 Substrate
40 Semiconductor Device
41 Package Supply Table
42 Stack Head
43A, 43B FURAKKU feed zone
44A-44E Imprint head
45 Camera Unit
46A, 46B Carrier stage
50 Flux
54A-54C FURAKKU spreading section
55 Positioning Fixture
57 Clip Member
58 Flux Loading Slot

[Translation done.]